IN THE CLAIMS

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1.   (Currently Amended) For use in a fixed-size packet switch, a switch fabric comprising:

N input buffers to receive incoming fixed-size data packets from an input port at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate, wherein said N input buffers are internal to said switch fabric and are external to said input port;

N output buffers to receive fixed-size data packets at said second data rate and to output said fixed-size data packets to an output port at said first data rate, wherein said N output buffers are internal to said switch fabric and are external to said output port; and

a bufferless, non-blocking interconnecting network to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate.

2.   (Original)   The switch fabric as set forth in Claim 1 wherein said bufferless, non-blocking interconnecting network comprises a bufferless crossbar.

3.   (Original)   The switch fabric as set forth in Claim 1 wherein each of said N input buffers is at least twice the size of each of said N output buffers.

4.   (Currently Amended) A method of operating a switch fabric in a fixed-size packet switch, the method comprising the steps of:

storing incoming fixed-size data packets <u>from input port</u> in N input buffers at a first data rate, wherein said N input buffers are internal to said switch fabric <u>and are external to said input port</u>;

outputting the fixed-size data packets from the N input buffers at a second data rate equal to at least twice the first data rate;

transferring the fixed-size data packets output by the N input buffers at the second data rate through a bufferless, non-blocking interconnecting network to N output buffers, wherein said N output buffers are internal to said switch fabric;

storing the fixed-size data packets transferred through the bufferless, non-blocking interconnecting network in the N output buffers at the second data rate; and

outputting the fixed-size data packets from the N output buffers at the first data rate <u>to an output port, wherein said output buffers are external to said output port</u> .

5.   (Original)   The method as set forth in Claim 4 wherein the bufferless, non-blocking interconnecting network comprises a bufferless crossbar.

6.   (Original)   The method as set forth in Claim 5 wherein each of the N input buffers

is at least twice the size of each of the N output buffers.

7.   (Currently Amended) A fixed-size data packet switch comprising:

N input ports to receive incoming fixed-size data packets at a first data rate and to output said

fixed-size data packets at said first data rate;

N output ports to receive fixed-size data packets at said first data rate and to output said

fixed-size data packets at said first data rate; and

a switch fabric interconnecting said N input ports and said N output ports comprising:

N input buffers to receive incoming fixed-size data packets <u>from at least one of said N input</u>

<u>ports</u> at said first data rate and to output said fixed-size data packets at a second data rate equal to at

least twice said first data rate, wherein said N ~~output~~ <u>input</u> buffers are internal to said switch fabric

<u>and are external to said N input ports</u>;

N output buffers to receive fixed-size data packets at said second data rate and to output said

fixed-size data packets at said first data rate <u>to said at least one of said N output ports</u>, wherein said

N output buffers are internal to said switch fabric <u>and are external to said N output ports</u>; and

a bufferless, non-blocking interconnecting network to receive from said N input buffers said

fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N

output buffers at said second data rate.

8.   (Original)   The fixed-size data packet switch as set forth in Claim 7 wherein said bufferless, non-blocking interconnecting network comprises a bufferless crossbar.

9.   (Original)   The fixed-size data packet switch as set forth in Claim 7 wherein each of said N input buffers is at least twice the size of each of said N output buffers.

10.   (Previously Presented)   The fixed-size data packet switch as set forth in Claim 7 further comprising a scheduling controller to schedule transfer of said fixed-size data packets from said N input ports to said switch fabric.

11.   (Previously Presented)   The fixed-size data packet switch as set forth in Claim 10 wherein said scheduling controller schedules transfer of said fixed-size data packets from said N output ports to an external device.

12.   (Previously Presented)   The fixed-size data packet switch as set forth in Claim 10 wherein said scheduling controller schedules transfer of said fixed-size data packets from said N input buffers to said bufferless, non-blocking interconnecting network.

13.   (Previously Presented)   The fixed-size data packet switch as set forth in Claim 12 wherein said scheduling controller schedules transfer of said fixed-size data packets from said N output buffers to said N output ports.

14.   (Currently Amended) A communication network to transfer data in fixed-size packets between a plurality of end-user devices, said communication network comprising:

a plurality of fixed-size data packet switches, at least one of said fixed-size data packet switches comprising:

N input ports to receive incoming fixed-size data packets at a first data rate and to output said fixed-size data packets at said first data rate;

N output ports to receive fixed-size data packets at said first data rate and to output said fixed-size data packets at said first data rate; and

a switch fabric interconnecting said N input ports and said N output ports comprising:

N input buffers to receive incoming fixed-size data packets at said first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate, wherein said N input buffers are internal to said switch fabric and are external to said N input ports;

N output buffers to receive fixed-size data packets at said second data rate and to output said fixed-size data packets at said first data rate, wherein said N output buffers are internal to said switch fabric and are external to said N output ports; and

a bufferless, non-blocking interconnecting network to receive from said N input buffers said

fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N

output buffers at said second data rate.

15.   (Original)   The communication network as set forth in Claim 14 wherein said

bufferless, non-blocking interconnecting network comprises a bufferless crossbar.

16.   (Original)   The communication network as set forth in Claim 14 wherein each of

said N input buffers is at least twice the size of each of said N output buffers.

17.   (Previously Presented)   The communication network as set forth in Claim 14

further comprising a scheduling controller schedules transfer of said fixed-size data packets from

said N input ports to said switch fabric.

18.   (Previously Presented)   The communication network as set forth in Claim 17

wherein said scheduling controller schedules transfer of said fixed-size data packets from said N

output ports to an external device.

19.   (Previously Presented)   The communication network as set forth in Claim 17

wherein said scheduling controller schedules transfer of said fixed-size data packets from said N

input buffers to said bufferless, non-blocking interconnecting network.

20.   (Previously Presented)   The communication network as set forth in Claim 19

wherein said scheduling controller schedules transfer of said fixed-size data packets from said N

output buffers to said N output ports.